IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Oct. 7 time-1
#9/B
Memo
2-29-00

PETITION FOR AN EXTENSION OF TIME AND AMENDMENT "B"

APPLICANT: Ohsawa et al

SERIAL NO.: 09/199,305 GROUP ART UNIT: 2811

DATE FILED: November 25, 1998 EXAMINER: L. Thai

INVENTION: "A SEMICONDUCTOR DEVICE AND AN ELECTRICAL DEVICE USING THE SEMICONDUCTOR DEVICE"

Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Applicants hereby petition the Assistant Commissioner for Patents for a one-month extension of time for responding to the Office Action dated October 15, 1999 and are enclosing a check for the $110.00 government fee so that the period of response is extended from January 15, 2000 to February 15, 2000.

In response to the Office Action dated October 15, 1999, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 2, line 8, change "does" to read --do--.

Page 4, line 16, change "sodium chloride" to read --semiconductor device--.

Page 5, lines 21 and 25, change "fining" (both occurrences) to read --fineness--

Page 6, line 8, delete "substrate, a mask film";

lines 9-12, delete these lines; and

line 13, delete "of the metal".

Page 9, line 1, delete "and";

line 4, change "CSP." to read --CSP; and

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Figure 8 is an enlarged cross-sectional view of the area in the chain line circle VIII of Fig. 1E.

Page 17, line 8, change the line to read --view of the electrode 6 (see Fig. 8),--;

line 9, delete "Fig. 1E,"; and

same line, after "depicted" insert --either in Fig. 1E or--.

Page 19, line 17, change "fining" to read --fineness--.

Page 22, line 9, change "finesse" to read --fineness--; and

line 14, change "Finesse" to read --Fineness--.

Page 24, line 23, change "16" to read --27--.

Page 26, line 1, after "resin" insert --16--.

IN THE CLAIMS:

Please add the following claims:

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--14. An electronic device according to claim 11, wherein the wiring films comprise two layers with a layer of nickel covering the layer of copper so that the wires are connected to the nickel layer.--

15. A semiconductor device according to claim 1, wherein the wiring films are formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer.

REMARKS

Clams 1-15 are presented for reconsideration.

In the Office Action, claims 6-10, which are directed to the method, were withdrawn from further consideration; the drawings were objected to by the Draftsperson and also Figs. 4A, 7A and 7B were objected to by the Examiner; claims 1-3 were rejected under 35 USC 102(e) on Chia et al; claims 1-3 were also rejected under 35 USC 102(e) as being anticipated by Distefano et al; claims 11 and 12 were rejected under 35 USC 103 as being unpatentable over Chia et al and/or Distefano et al; claims 4 and 13 were rejected under 35 USC 103 as being unpatentable over Chia et al and/or Distefano et al in further view of McCormick et al; claim 5 was rejected under 35 USC 103 as being unpatentable over Chia et al in view of Shim et al and applicants note that U.S. Patents to Yano et al and Freyman et al were cited, but not applied.

Attached herewith is a letter proposing drawing changes, which designates the portion of Fig. 1E as Fig. 8, as indicated in red, to overcome the Draftsperson's objection to Fig. 1E; corrects the spelling of "electrode" in Figs. 4A and 4B; provides the base 5 in Fig. 4C, as indicated in red; adds element number 27 to Figs. 5D, 5E and 5F; adds element number 16 to Figs. 5I and 5J and provides the label "Prior Art" for Figs. 4A, 7A and 7B. If these corrections are approved, Formal Drawings incorporating these changes will be submitted once the application has been allowed.

By this amendment, typographical errors have been corrected in the specification; a description of Fig. 8 has been added and claims 14 and 15 have been added to further describe the film, such as illustrated in Fig. 1A-1I.

As pointed out in applicants' disclosure, the semiconductor device can be used in an electrical device and has a base 5 which has wiring films embedded in an upper surface so that the upper surface of the film is coplanar with the surface of the base and this upper surface receives the semiconductor element. In one embodiment, each of the wiring films is formed of two layers, with the upper layer being a nickel layer to facilitate the bonding of the wires 15 to that layer, such as the layer 3. In the other embodiment, the films are a single layer. Each of the films overlaps an electrode-forming hole which receives a conductive metal that forms a contact on a back or lower surface of the base opposite to the surface receiving the semiconductor element.

It is respectfully submitted that the rejections of claims 1-3 on Chia et al are in error and should be withdrawn for the following reasons. Contrary to the Examiner's description of this reference, the substrate 10 is that portion in cross-hatching in Fig. 2, and it is submitted that the contact films, such as 16 and 14, do not lie in the plane of the substrate. It is noted that the portion that the Examiner indicates as 10" is a solder mask layer 22 which protects the bottom surface of the substrate from solder. It is thus submitted that, contrary to the Examiner's discussion, the reference does not teach or suggest a base of an insulating resin have electrode-forming holes, the surface of the wiring films and the surface of the base being positioned on the same plane and that the semiconductor element is positioned on the front surface of the base with an insulating film therebetween. Therefore, it is submitted that Chia et al does not anticipate or even render obvious applicants' invention, as recited in clams 1-3, and that the rejections based on Chia et al in combination with other references, for claims 4, 5 and 11-13, are clearly in error and should be withdrawn. It is also noted that Chia et al does not teach or suggest that the films are a two-layer system with the outer surface of the two layers being the nickel layer. Thus, it is submitted that newly-added claims 14 and 15 are clearly patentable over Chia et al and any combination of the references of record.

With regard to Distefano et al, it is submitted that in Figs. 3F and 3G, the substrates are 30, 35 and 110, as described by the reference; that the terminals 40, while

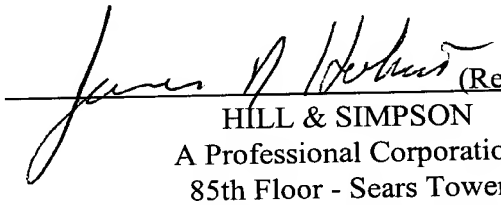
appearing to be embedded in some type of material, are not described. Even if the portion identified as 30' by the Examiner were the base, the upper surface of this base does not have the semiconductor element mounted thereon. It is submitted that there is no teaching or suggestion of applicants' claimed base without relying on applicants' disclosure to suggest the necessary modifications and interpretations of this reference. Thus, it is submitted that the rejections based on this reference should be withdrawn, since the Examiner has misconstrued and misdescribed the teachings of this reference.

It is also noted that, contrary to the Examiner's statement, Shim et al does not teach or suggest vents, since the holes 23 are plated through-holes, and it is submitted that it would not be the vents, such as recited in claim 5.

In summary, it is submitted that claims 1-5 and 11-15 are patentable over the references of record and are allowable.

In view of the amendments and explanations contained hereinabove, it is respectfully submitted that this application is now in condition for immediate formal allowance and further reconsideration to that end is earnestly solicited.

Respectfully submitted,



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DATED: February 15, 2000